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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/646,922 | 08/25/2003 | Masami Makino | 031057. | 1951 |

23850 7590 02/09/2007

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

| EXAMINER | |
|---|---|
| SAMS, MATTHEW C | |
| **ART UNIT** | **PAPER NUMBER** |
| 2617 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 02/09/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/646,922 | MAKINO ET AL. | |
| | Examiner | Art Unit | |
| | Matthew C. Sams | 2617 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This office action is in response to the amendment filed on 11/20/2006.

2. The examiner thanks the applicant for providing the translation of JP 59-78654.

### *Response to Arguments*

3. Applicant's arguments filed 11/20/2006 have been fully considered but they are not persuasive.

4. In response to the applicant's argument regarding claim 1 that there is no motivation to combine because "Kweon specifically teaches LCD panels separated by a light guide plate" and that the chip mount areas are not "positioned directly next to each other" (Pages 3-4), the examiner disagrees.

Kweon shows in (Fig. 3 [LCD 27]) a chip between two mounting holes that is located on a second parallel plane above the LCD [27]. Kweon teaches the same alignment of two mounting holes, but with a hole in place of the chip in (Fig. 3 [25]). Kweon teaches the light guide plate (Fig. 3 [23]) can clearly be inserted into the frame (Fig. 3 [24]) as seen by the contour along the inside of the frame. (Col. 3 lines 59-60) Kweon teaches the combination of [23 & 24] is inserted into the LCD [27], between the microchip with mounting holes and the LCD [27]. (Col. 3 lines 59-67) Kweon teaches the PCB [25] mounts to the frame [24] through the holes that are in the respective top left and right corners. Therefore, when the second LCD [28] is attached to the PCB [25], it would be obvious to one of ordinary skill in the art to use the teachings of JP 59-

78654 to stagger the mounting locations of the chips to make the configuration thinner because the chips are directly next to each other in an opening of a frame.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kweon et al. (US-6,925,313 hereafter, Kweon) in view of the cited prior art document JP 59-78654, hereafter document 59-78654.

Regarding claims 1 and 2, Kweon teaches a foldable electronic device (Fig. 1 [10] & Fig. 2 [20]) comprising a main body (Fig. 1 [10A]), a closure (Fig. 1 [10B]), a main display (Fig. 1 [12]), a subdisplay (Fig. 2 [22B]), a frame (Fig. 3 [24]), a chip mount area extending from the main display (Fig. 3 [27]) and a chip mount area extending from the subdisplay (Fig. 3 [28]). Kweon teaches the main body (Fig. 1 [10A]) and the closure (Fig. 1 [10B]) being connected to each other openably (Fig. 1 & 2), with the main display (Fig. 1 [12]) having a screen exposed from an inner surface of the closure (Fig. 1) and the subdisplay (Fig. 2 [22B]) having a screen exposed from the back surface of the closure (Fig. 2), the frame (Fig. 3 [24]) being provided inside the closure (Fig. 5 [21, 22 & 24] and Col. 2 lines 48-50) and securing the main display and the subdisplay as arranged back to back (Fig. 1, Fig. 2, Fig. 3 and Col. 2 lines 40-42) with the chip mount

areas being opposed to each other in an opening formed in the frame (Fig. 3) with the opposed surfaces of the respective chip mount areas having groups of electronic chips mounted thereon. (Fig. 3 [27 & 28] & Fig. 5) Kweon teaches the chip mounting surfaces has a folded-over portion opposed to the frame and providing the chip mounting area. (Fig. 3 [28]) Kweon differs from the claimed invention by not explicitly reciting the groups of electronic circuit chips are positioned in a staggered relation to each other and mounted on flexible leads.

In an analogous art, document 59-78654 teaches a flexible circuit board where taller and shorter groups of chips are mounted in a staggered relation to each other. (Claim 1, Page 3 lines 10-20 and Fig. 3) At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement the LCD mounting arrangement of Kweon after modifying it to incorporate the flexible chip mounting surface and the staggered chip-mounting pattern of document 59-78654. One of ordinary skill in the art would have been motivated to do this since making portable electronic devices thinner allows them to be more convenient for the consumer to carry.

Regarding claim 3, Kweon in view of document 59-78654 teaches a foldable electronic device with a frame that has an opening in a second area (Fig. 3 [24]) adjacent to a first area covered with the subdisplay and the flexible lead extending from the subdisplay is folded over ion the second area with the electronic chips in the chip mount area being positioned in the opening of the frame. (Fig. 3)

Regarding claim 4, Kweon in view of document 59-78654 teaches a flexible lead (Kweon Fig. 3 [25 & 27] & document 59-78654 Fig. 3) extending from the main display (Fig. 3 [27]) is folded over toward the frame side and folded-over lead portion has a

surface opposed to the frame and providing the chip mount area, the electronic circuit chips in the chip mount area being positioned in the opening of the frame. (Fig. 3)

Regarding claim 5, Kweon in view of document 59-78654 teaches a flexible lead (Kweon Fig. 3 [25 & 28] & document 59-78654 Fig. 3) extending from the subdisplay (Fig. 3 [28]), has an outer end folded over toward the frame side and folded-over portion has a surface opposed to the frame and providing the chip mount area. (Fig. 3)

Regarding claim 6, Kweon in view of document 59-78654 teaches a foldable electronic device with a frame that has an opening in a second area (Fig. 3 [24]) adjacent to a first area covered with the subdisplay and the flexible lead extending from the subdisplay is folded over ion the second area with the electronic chips in the chip mount area being positioned in the opening of the frame. (Fig. 3)

Regarding claim 7, Kweon in view of document 59-78654 teaches a flexible lead (Kweon Fig. 3 [25 & 27] & document 59-78654 Fig. 3) extending from the main display (Fig. 3 [27]) is folded over toward the frame side and folded-over lead portion has a surface opposed to the frame and providing the chip mount area, the electronic circuit chips in the chip mount area being positioned in the opening of the frame. (Fig. 3)

## *Conclusion*

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Sams whose telephone number is (571)272-8099. The examiner can normally be reached on M-F 7:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester Kincaid can be reached on (571)272-7922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MCS
1/31/2007

LESTER G. KINCAID
SUPERVISORY PRIMARY EXAMINER